

FLASH MEMORY WITH LOW TUNNEL BARRIER INTERPOLY  
INSULATORS

Abstract of the Disclosure

5 Structures and methods for Flash memory with low tunnel barrier intergate  
insulators are provided. The non-volatile memory includes a first source/drain  
region and a second source/drain region separated by a channel region in a substrate.  
A floating gate opposing the channel region and is separated therefrom by a gate  
oxide. A control gate opposes the floating gate. The control gate is separated from  
10 the floating gate by a low tunnel barrier intergate insulator. The low tunnel barrier  
intergate insulator includes a metal oxide insulator selected from the group  
consisting of PbO, Al<sub>2</sub>O<sub>3</sub>, Ta<sub>2</sub>O<sub>5</sub>, TiO<sub>2</sub>, ZrO<sub>2</sub>, and Nb<sub>2</sub>O<sub>5</sub>. The floating gate includes  
a polysilicon floating gate having a metal layer formed thereon in contact with the  
low tunnel barrier intergate insulator. And, the control gate includes a polysilicon  
15 control gate having a metal layer formed thereon in contact with the low tunnel  
barrier intergate insulator.

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